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Amendments to the drawings:

The attached sheet of drawings includes changes to FIG. 3B, in which the labels "yes" and "no" for reference number S208 have been corrected. No new matter is added.

Attachment: Replacement Sheet

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REMARKS

Claims 1-9 and 11-14 are pending in the application. Claim 1 has been amended to overcome the rejections under 35 USC 112, but is not otherwise amended. Claim 9 has been amended to incorporate the subject matter of claim 10, which has been canceled without prejudice. The amendments are fully supported by the application as originally filed.

The specification was objected to because of informalities on page 9, lines 4 and 11. The specification has been amended in the manner recommended by the Examiner to correct the inadvertent errors. No new matter is added. Approval of the corrected specification is respectfully requested.

Claims 1-8 were rejected under 35 USC 112, second paragraph as being indefinite because of antecedent basis issues. Claim 1 has been amended to provide proper antecedence for the language highlighted by the Examiner. It is believed that the amended claims overcome the rejection under 35 USC 112, second paragraph.

Claim 1 was rejected under 35 USC 112, first paragraph due to lack of enablement of claim 1, step (2). Claim 1, step (2) as originally filed includes the correct language. The specification has been amended on page 10, and step S208 of FIG. 3B has been corrected in the manner provided in original claim 1, step (2). No new matter is added. Regarding the additional rejection of claim 1, step (3), the step has been amended in the manner recommended by the Examiner (see, e.g., specification at page 11, first paragraph). No new matter is added. Withdrawal of the rejections under 35 USC 112, first paragraph is respectfully requested.

Applicant's claimed invention is directed to a method and system for calculating dynamic burst length, which can increase main memory unit bus resource usage efficiency, and avoid abnormal system operations caused when the length of a data byte exceeds the size of a main memory capacity (see, e.g., specification at page 5, second paragraph).

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As recited in claim 1, the method includes a step of: "(3) determining via a data length calculating module whether a sending data byte is the end of the packet data; if no, repeating step (3); if yes, calculating the length of this data byte" (see claim 1, step (3), emphasis added).

Moreover, the method of claim 1 recites a write-in index address that is added by one when a data byte is written to a buffering memory unit, and a read-out index address that is added by one when a data byte is read out from the buffering memory unit (claim 1, step (1)). In other words, both the write-in index address and the read-out index address are incremented by one when a data byte is written to and read out from the buffering memory unit.

As amended, independent claim 9 recites a dynamic burst length calculating system including a burst length determining module, a data length calculating module, and a valid data calculating module. Specifically, independent claim 9 recites "a data length calculating module controlled by the network communication system module, and for calculating the length of a data byte waiting to be transferred for the dynamic burst length calculating system" (claim 9).

Claims 1-14 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 6,397,287 to Brown et al. ("Brown"). This rejection is respectfully requested.

Brown does not teach or suggest a method for calculating dynamic burst length including the step of: "(3) determining via a data length calculating module whether a sending data byte is the end of the packet data; if no, repeating step (3); if yes, calculating the length of this data byte" (see claim 1, step (3), emphasis added).

Similarly, Brown does not teach or suggest the Applicant's claimed system, including: "a data length calculating module controlled by the network communication system module, and for calculating the length of a data byte waiting to be transferred for the dynamic burst length calculating system" (claim 9).

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Brown discloses the use of "RxFree" 66 and "RxUsed" 67 registers, where "RxFree" represents the current amount of free space in the receive buffer 25, and RxUsed represents the amount of packet data currently in the receive buffer 25" (column 14, lines 28-31; and FIGS. 6(a) to 6(c) of Brown). In Brown, the RxFree and RxUsed registers are complementary (see column 14, lines 34-36). For example, when data is written to the receive buffer 25 in Brown, the RxUsed register is incremented, while the RxFree register is decremented (i.e., the RxUsed and RxFree registers move in opposite directions).

In contrast, the Applicant's claimed invention requires a write-in index to be incremented ("adding a write-in index address in a register by one") when a data byte is written to a buffering memory unit, and a read-out index to be incremented ("adding a read-out index in the register by one") when a data byte is read out from the buffering memory unit.

For at least the reasons discussed above, the Brown reference does not anticipate or otherwise render obvious the Applicant's claimed invention.

It is believed that the claims are in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



Peter F. Colless (Reg. No. 33,860)
Steven M. Jensen (Reg. No. 42,693)
Edwards Angell Palmer & Dodge
P.O. Box 55874
Boston, MA 02205

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Phone: (617) 439-4444

Customer No. 21874